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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,661	07/26/2001	Harm Peter Hofstee	AUS920010307US1	7329

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	6

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,661	HOFSTEE ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been presented for examination.

Claim Objections

2. Claim 20 is objected to because of the following informalities: Claim 20 is dependent upon itself. For examining purposes, it has been interpreted that Claim 20 is dependent upon claim 17. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-8, 10, 14, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Buller et al[1] [Buller] US Pat No 5737171

5. Referring to claim 1, Buller teaches the apparatus for reducing the rate of temperature change in a processing device due to a change in operational state for the processing device including:

a. a power transitioning arrangement for transitioning power dissipation in the processing device between a low power dissipation level and a high power dissipation level in response to a change in a power state signal, the high power dissipation level being relatively greater than the low power dissipation level [abstract].

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[1] As cited by the applicant

b. a cooling system alternatively providing a low thermal impedance for the processing device and a relatively higher, high thermal impedance for the processing device [abstract].

c. a cooling system controller for placing the cooling system at the high thermal impedance in conjunction with a transitioning from the high power dissipation level to the low power dissipation level, and for placing the cooling system at the low thermal impedance in conjunction with a transitioning from the low power dissipation level to the high power dissipation level [abstract].

6. Referring to claim 6, Buller teaches a high power level corresponding to a maximum clock rate and a minimum power level corresponding to a sleep clock rate [fig. 3 and col. 3 lines 47-57].

7. Referring to claim 7, Buller teaches that the cooling system comprises a heat sink and a fan positioned over the heat sink [fig. 1].

8. Referring to claim 8, the RUN/SLEEP signal is interpreted as an awake/asleep signal [col. 3 lines 49-51]. In addition, it is inherent that the cooling system would be powered by a system power supply and that the system power would be supplied to the cooling system when the system is active and not supplied to when the cooling system is off. This is also interpreted as a power on/off signal for a processing device.

9. Referring to claim 10, Buller teaches the invention substantially including:

a. transitioning from a high power state to a low power state in response to a change in a high power state signal to a low power state signal and also for transitioning from a

low power state to a high power state in response to a change in a low power state signal to a high power state signal [abstract].

b. a cooling system providing alternate thermal impedance states for transferring heat from the processing system, the thermal impedance states including a high thermal impedance state and a relatively lower, low thermal impedance state [abstract].

c. a cooling system controller operably connected to the cooling system for changing the thermal impedance state of the cooling system from the high thermal impedance state to the low thermal impedance state in response to a change from the low power state signal to the high power state signal, and for changing the thermal impedance state of the cooling system from the low thermal impedance state to the high thermal impedance state in response to a change from the high power state signal to the low power state signal [abstract].

Although Buller does not explicitly teach that the transitioning between a high and low power mode is directly related to transitioning between a high and low speed clock rate, Buller teaches that clock rate is directly related to performance and power dissipation [col. 1 lines 21-29]. Because the Buller system transitions between a high and low power state and because Buller teaches that clock rate is directly related to performance and power dissipation, it is inherent in the Buller system that a transition to a high power state would include transitioning the system clock to a high clock rate and that a transition to a low power state would include transitioning the system clock to a low clock rate.

9. Referring to claims 14 and 15, these are rejected on the same basis as set forth hereinabove.

10. Referring to claim 17, this is rejected on the same basis as set forth hereinabove. Buller teaches the apparatus performing the method and therefore teaches the method itself.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buller as applied to claims 1, 6-8, 10, 14, 15 and 17 above, and further in view of Thomas et al [Thomas] US Pat No 5752011.

13. Referring to claim 2, even though Buller teaches a cooling system for applying either high or low thermal impedance to a circuit, it is taught by Thomas that systems can still overheat [col. 2 lines 15-16]. Therefore, Buller does not explicitly teach delaying a transition between power levels relative to a change between a low and high thermal impedance. Thomas teaches that a change in the thermal impedance should occur before a transition in the power state. Doing this would allow a high power mode to be sustained for a longer period of time thus inherently delaying a reduction in frequency due to high temperature [col. 8 lines 50-56]. It would have been obvious to one of ordinary skill in the art to include the teachings of Thomas into the Buller system because it would provide a means to prevent overheating of the Buller system while still providing a means to maintain a high power mode for as long as possible.

14. Referring to claims 11 and 18, these are rejected on the same basis as set forth hereinabove.

15. Claims 4, 9, 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buller as applied to claims 1, 6-8, 10, 14, 15 and 17 above and further in view of Kim US Pat No 6009005.

16. Referring to claim 4, Kim teaches that the input clock can be output from the frequency divider without being divided [col. 6 lines 2-4]. This is interpreted as a frequency divider bypass because the frequency divider is directly outputting the clock without operating on it. Furthermore, it is obvious that the clock in the Buller-Kim system is a system clock because it is being used to put the system into either a high power mode or a low power mode.

17. Referring to claim 9, it is obvious that when the bypass signal is received, that the Buller-Lee system would operate at a high power level substantially immediately due to the fact that the output clock from the frequency divider would be at a maximum rate. The bypass signal is interpreted as being the signal sent to the frequency divider (128) from the controller (126) in Lee.

18. Referring to claims 12 and 16, these are rejected on the same basis as set forth hereinabove.

19. Claims 3, 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buller as applied to claims 1, 6-8, 10, 14, 15 and 17 above, and further in view of Bailey et al [Bailey] US Pat No 6654898.

20. Referring to claims 3 and 5, although Buller teaches a system for reducing heat on integrated circuit packages (IC) within a host system, wherein the host system has different power modes; Buller is not specific on any details regarding the host system. Bailey teaches that communication within the host system must occur wherein different IC's within the host system operate using different clocks [col. 1 lines 21-31]. Bailey teaches a means to produce the required clock frequencies using a plurality of clock dividers and dividing a system clock [figs. 1 and 2A and col. 5 lines 4-9]. Bailey further teaches a controlling means to control the clock signals depending on a certain power state [206 fig. 2A]. It would have been obvious to include the teachings of Bailey into the Buller system because it provides a way for the IC's in the Buller system to communicate while still maintaining compatibility with different power modes.

21. Referring to claim 13, this is rejected on the same basis as set forth hereinabove.

22. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buller as applied to claims 1, 6-8, 10, 14, 15 and 17 above, and further in view of Ganfield et al [Ganfield] US Pat No 5815694.

23. Referring to claim 19, Buller teaches transitioning between different power modes, wherein each power mode is related to a particular clock rate, as explained above. In summary, Buller teaches that a clock is adjusted in response to a change in the power mode. Buller though does not explicitly teach how the clock is transitioned. Ganfield explicitly states that a clock has to be transitioned gradually in order to "avert adverse consequences" [col. 1 lines 32-35]. Therefore it would be obvious to transition the clock in the Buller system gradually in order to avoid any adverse consequences associated with adjusting a clock frequency.

24. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buller as applied to claims 1, 6-8, 10, 14, 15 and 17 above, and further in view of Lee et al [Lee] US Pat No 5414863.

25. Referring to claim 20, it is well known in the art that computer systems comprises a plurality of processing elements and it is interpreted that the Buller system is no exception. Although Buller teaches the system transitioning between different power modes, it is not explicitly taught the process of transitioning an entire system into a different power mode. Lee teaches that different portions of the system should be transitioned in different stages to avoid power surges, damaging due to incorrect biasing and to decrease power usage [abstract, col. 4 lines 55-56 and col. 6 lines 3-10]. It would have been obvious to one of ordinary skill in the art to modify the power dissipation of the different processing elements at different times in order to minimize power surges and damaging to components due to incorrect biasing and to minimize power usage as taught by Lee.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (703) 305-7849. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
August 2, 2004

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